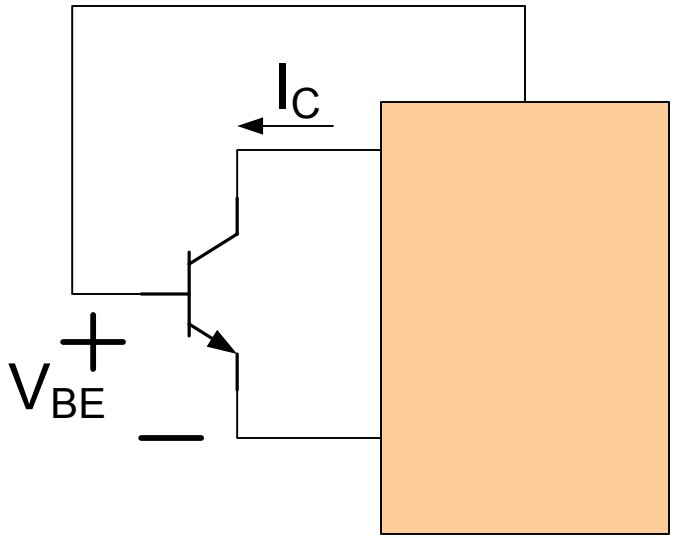
EE 434
Lecture 23

Models for Computer Simulation
Bipolar Small Signal Device Models

Quiz 15

The collector current IC was accurately measured to be 1.5mA and the V_{BE} was measured to be 0.65V. What is the J_S for the process if the emitter area is $100u^2$? Assume operation at room temperature.



And the number is ….

1 8 7 5 3

6 9 4 2

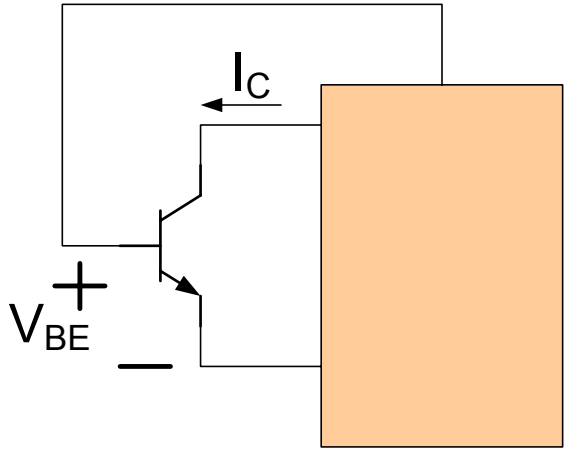
And the number is ….

1 8 7 5 3

6 9 4 2

Quiz 15

The collector current IC was accurately measured to be 1.5mA and the V_{BE} was measured to be 0.65V. What is the J_S for the process if the emitter area is $100u^2$? Assume operation at room temperature.



Solution:

$$I_C = J_S A_E e^{\frac{V_{BE}}{V_t}}$$

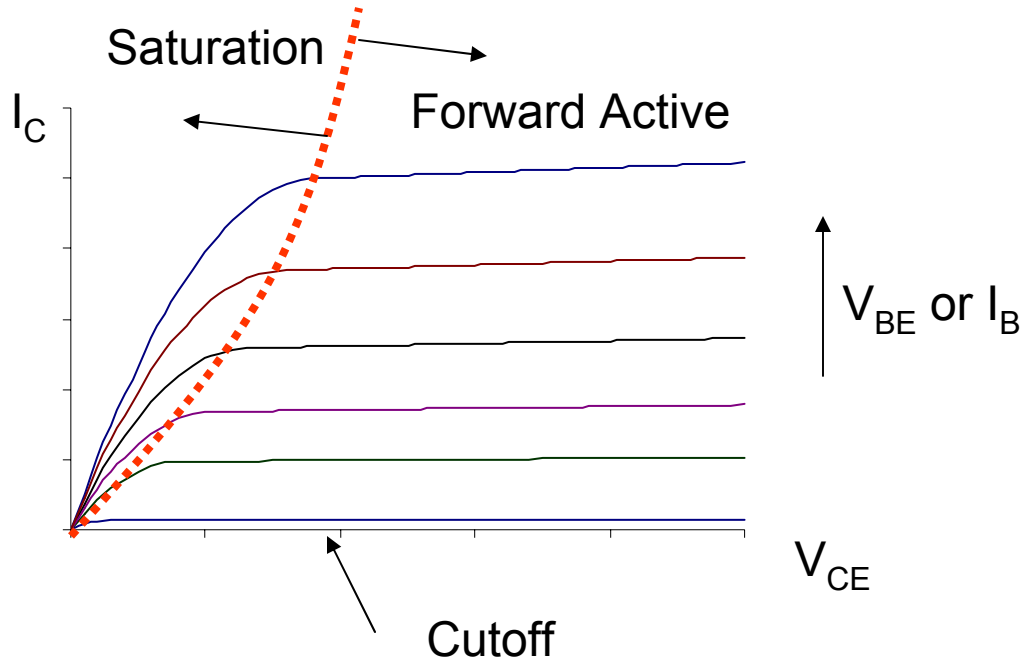
$$J_s = \frac{I_C}{A_E} e^{\frac{-V_{BE}}{V_t}}$$

$$J_s = \frac{1.5\text{mA}}{100\mu^2} e^{\frac{-.65\text{V}}{26\text{mV}}} = 2.08\text{E}-16\text{A}/\mu^2$$

Review from Last Time

Simple dc model

Typical Output Characteristics

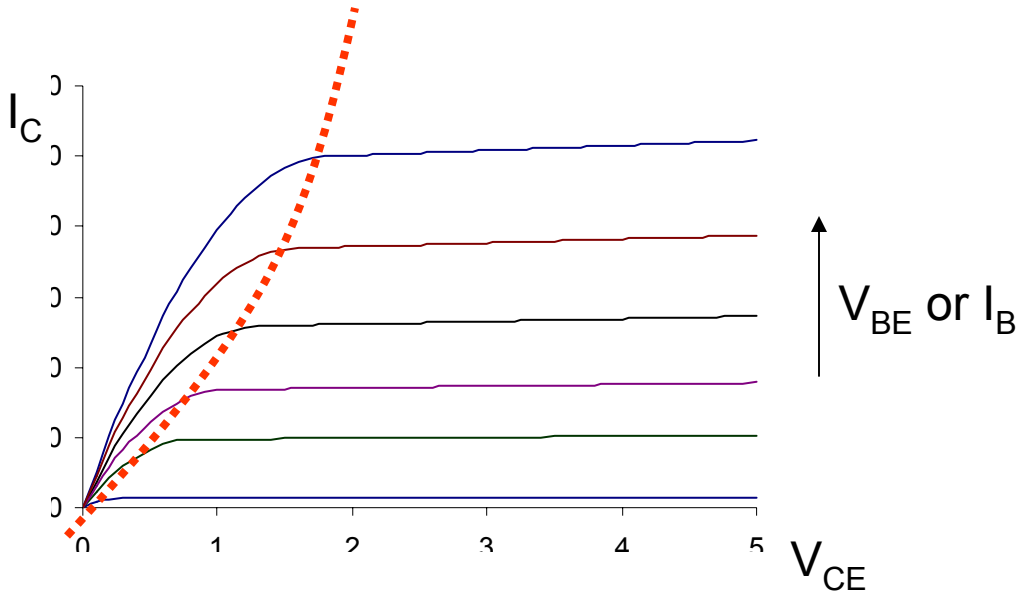


Forward Active region of BJT is analogous to Saturation region of MOSFET

Saturation region of BJT is analogous to Triode region of MOSFET

Review from Last Time

Improved dc model



$$V_t = \frac{kT}{q}$$

$$I_E = -\frac{J_S A_E}{\alpha_F}\left(e^{\frac{V_{BE}}{V_t}} - 1\right) + J_S A_E\left(e^{\frac{V_{BC}}{V_t}} - 1\right)$$

$$I_C = J_S A_E\left(e^{\frac{V_{BE}}{V_t}} - 1\right) - \frac{J_S A_E}{\alpha_R}\left(e^{\frac{V_{BC}}{V_t}} - 1\right)$$

Valid in All regions of operation

V_{AF} effects can be added

Not mathematically easy to work with

Note dependent variables changes

Termed Ebers-Moll model

Reduces to previous model in FA region

Review from Last Time

Simple dc model

Simplified Multi-Region Model

$$I_C = J_S A_E e^{\frac{V_{BE}}{V_t}}\left(1+\frac{V_{CE}}{V_{AF}}\right)$$

$$I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}}$$

$$V_t = \frac{kT}{q}$$

V_{BE}>0.4V

V_{BC}<0

Forward Active

V_{BE}=0.7V
V_{CE}=0.2V

I_C<βI_B

Saturation

I_C=I_B=0

V_{BE}<0

V_{BC}<0

Cutoff

A small portion of the operating region is missed with this model but seldom operate in the missing region

Review from Last Time

Simple dc model

Equivalent Simplified Multi-Region Model

$$I_C = \beta I_B \left(1 + \frac{V_{CE}}{V_{AF}}\right)$$

$$I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}}$$

$$V_t = \frac{kT}{q}$$

V_{BE}>0.4V

V_{BC}<0

Forward Active

V_{BE}=0.7V
V_{CE}=0.2V

I_C<βI_B

Saturation

I_C=I_B=0

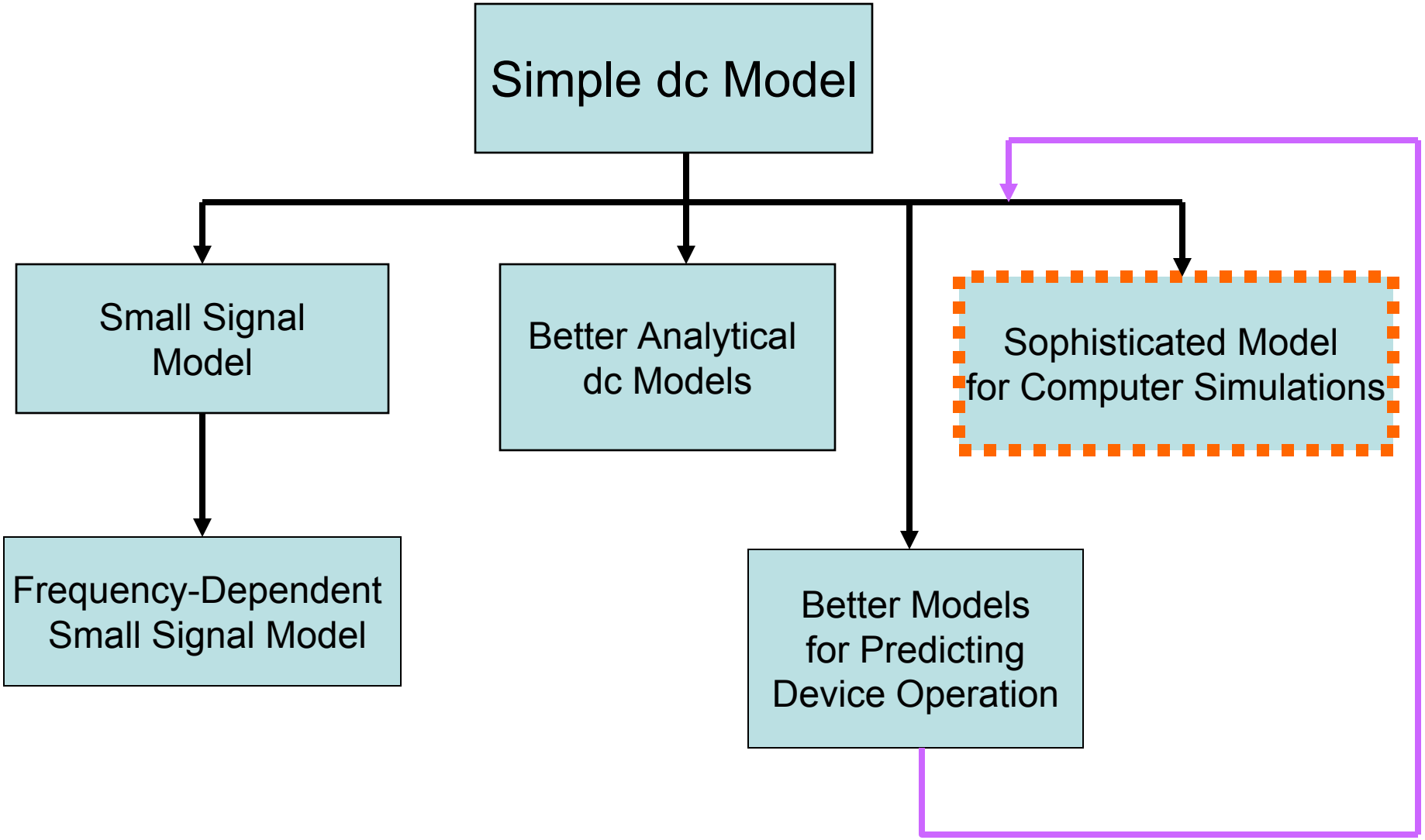
V_{BE}<0

V_{BC}<0

Cutoff

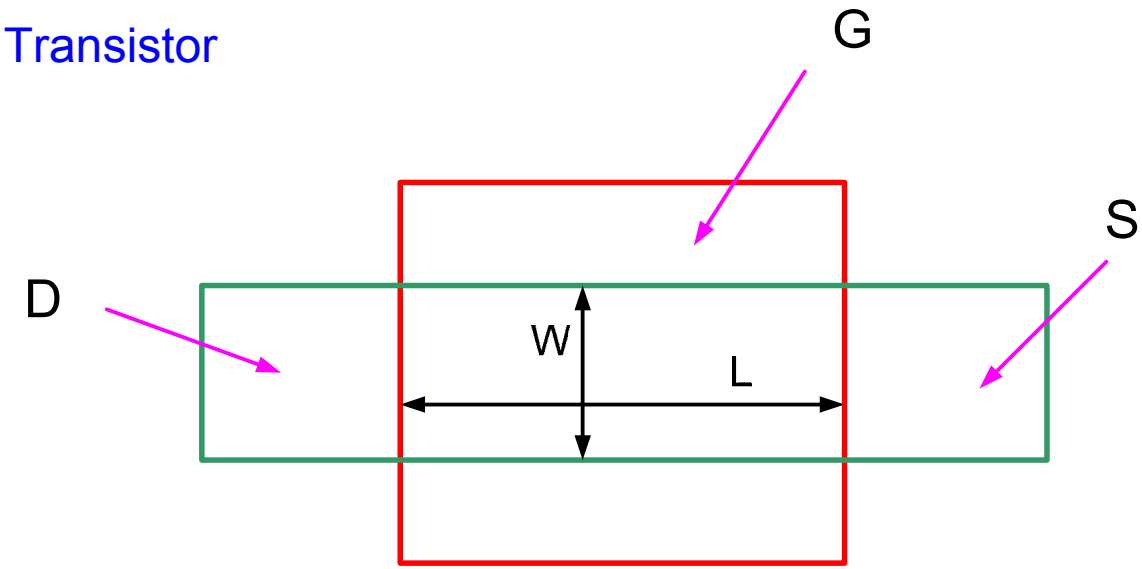
A small portion of the operating region is missed with this model but seldom operate in the missing region

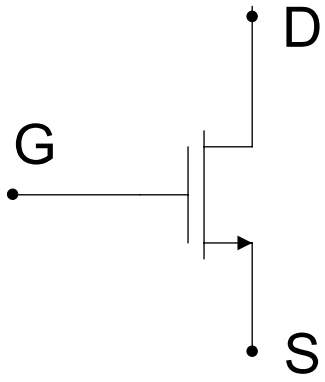
Models for Computer Simulation



Models for Computer Simulation

MOS Transistor





Model Parameters

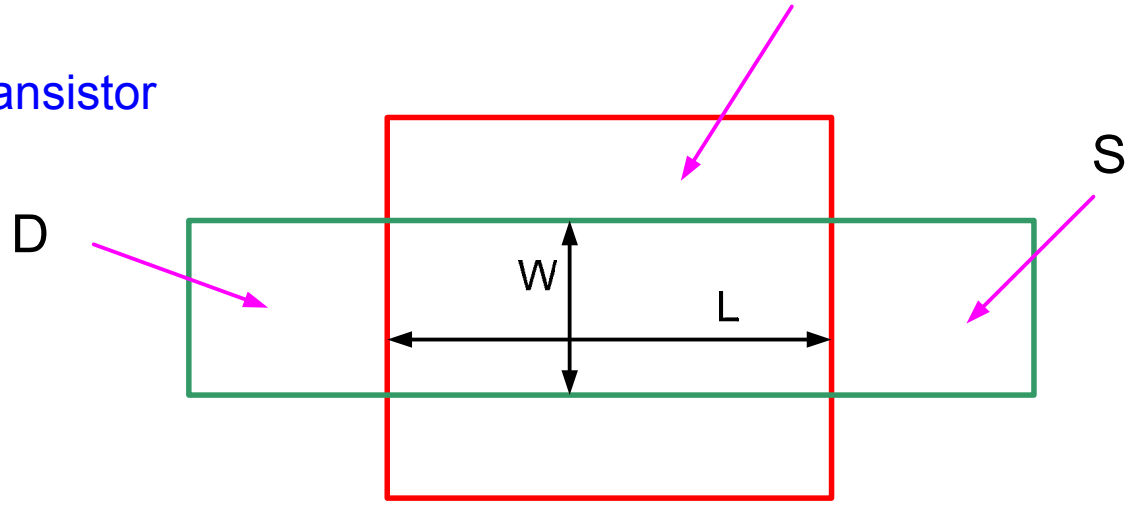
$$\{W, L, C_{GS}, C_{GD}, C_{GB}, C_{DB}, C_{SB}\}$$

Physical Parameters

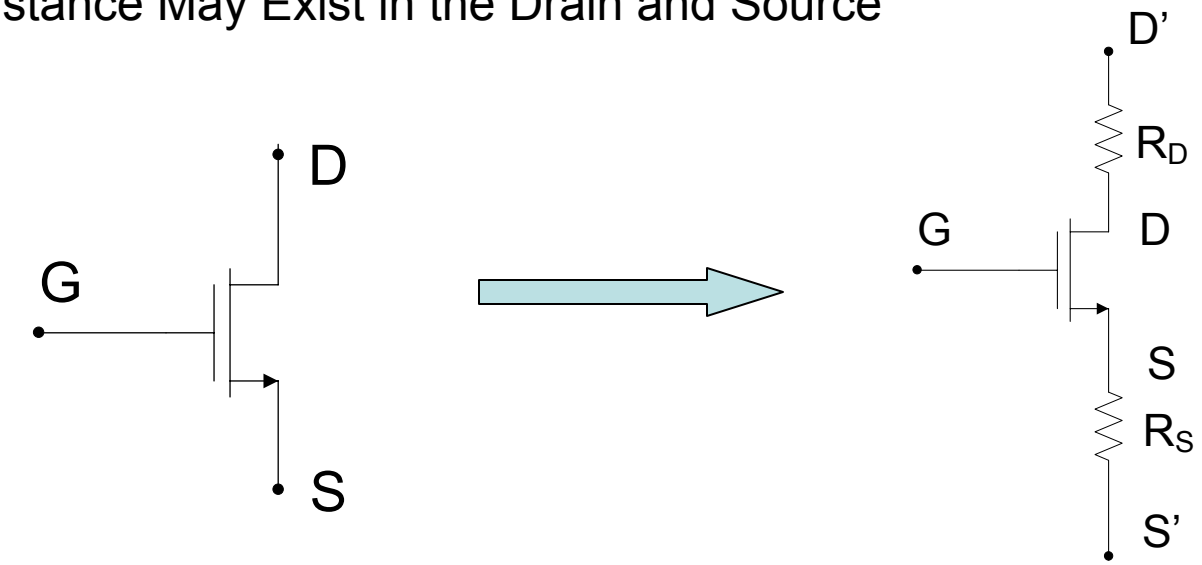
$$\{W, L, A_S, A_D, P_S, P_D\}$$

Models for Computer Simulation

MOS Transistor



Resistance May Exist in the Drain and Source

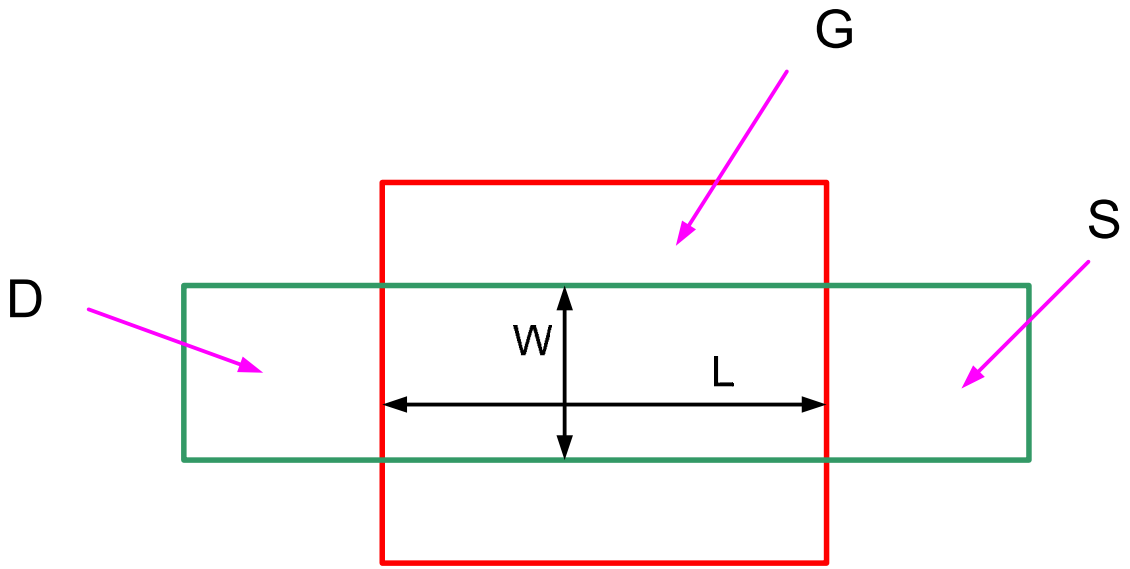


Models for Computer Simulation

MOS Transistor

Resistance May Exist in the Drain and Source

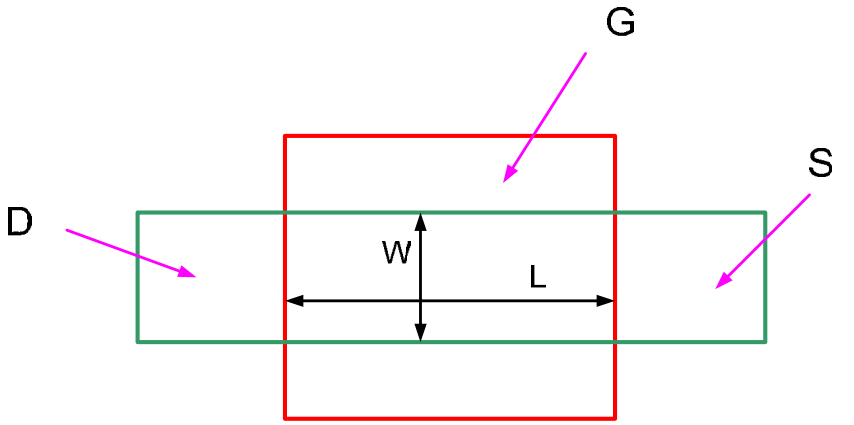
Where is the drain and the source D’ and S’?

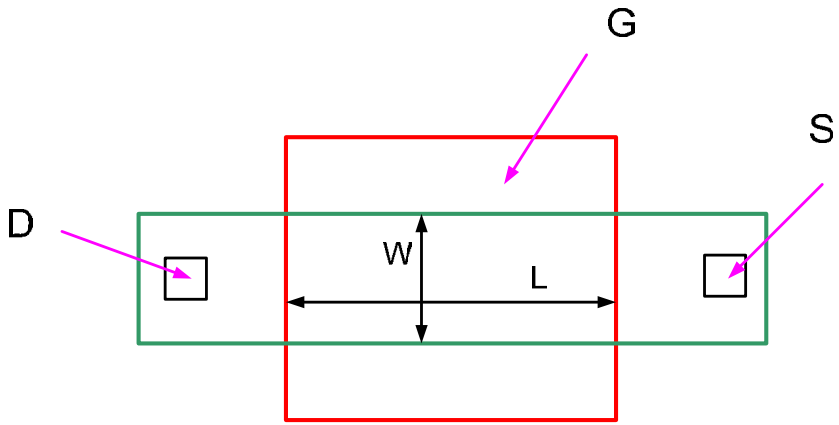


Models for Computer Simulation

MOS Transistor

Where is the drain and the source D' and S'?

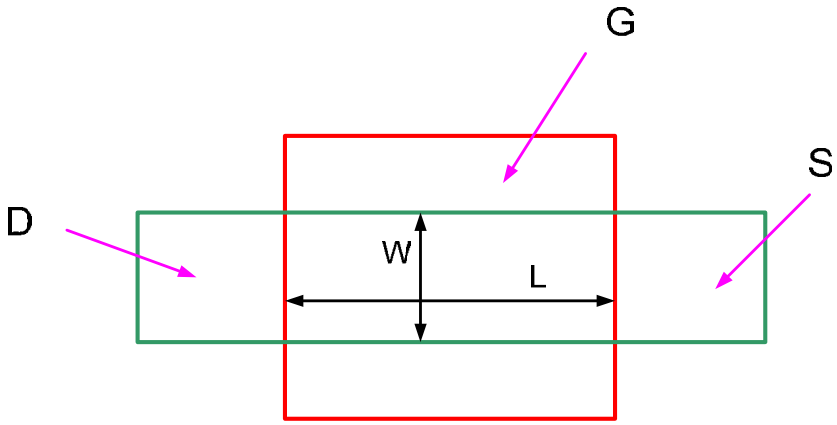


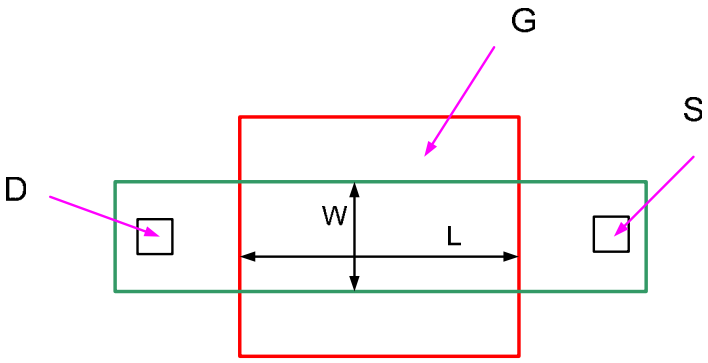


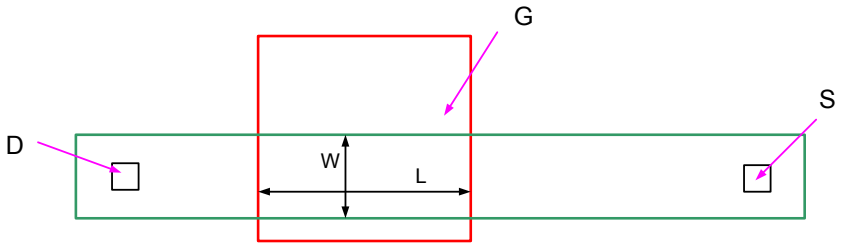
Models for Computer Simulation

MOS Transistor

Where is the drain and the source D' and S'?





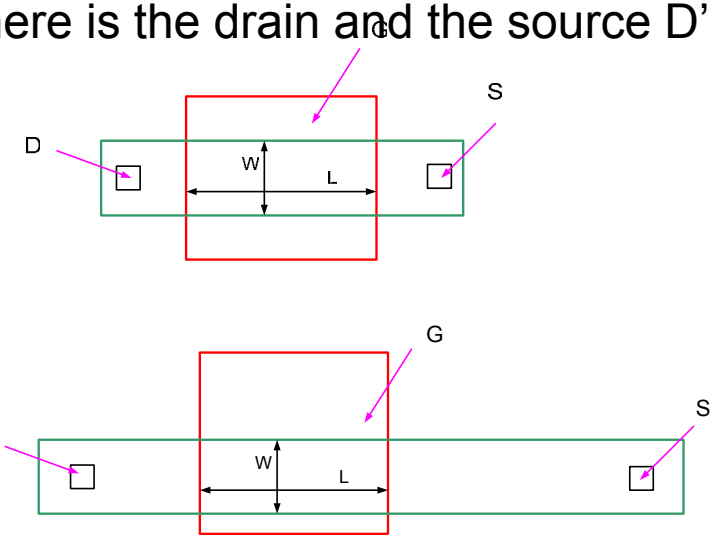


Considerable Interconnect may be made with diffusions

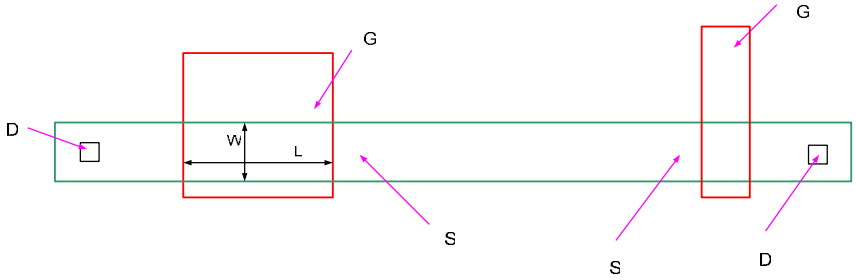
Models for Computer Simulation

MOS Transistor

Where is the drain and the source D' and S'?



Considerable Interconnect may be made with diffusions

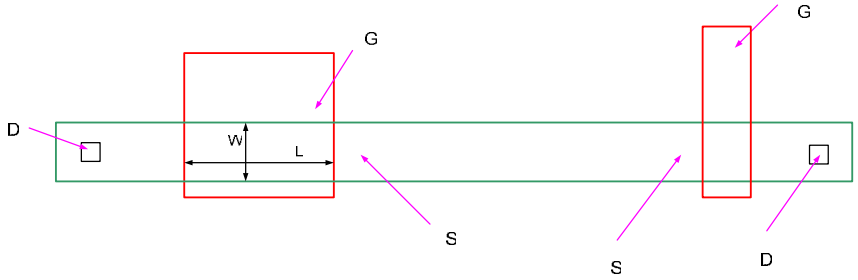


Drain and source boundary assignments is not unique !!

Models for Computer Simulation

MOS Transistor

Where is the drain and the source D' and S'?



Drain and source boundary assignments is not unique !!

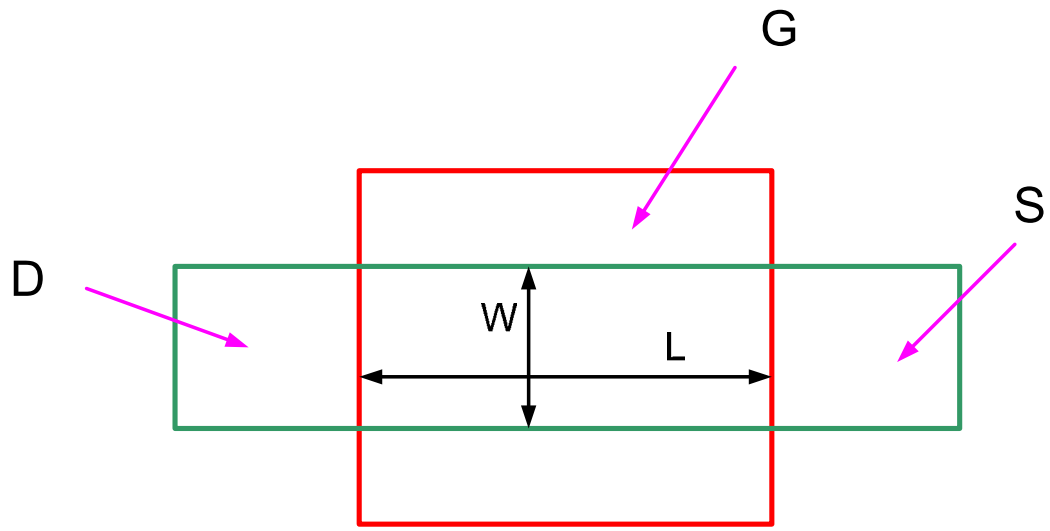
So, how are boundary assignments made?

However you want !!

But eventually must either include all parasitics as either part of devices or as parts of interconnects

Models for Computer Simulation

MOS Transistor



Model Parameters

$$\{W, L, R_S, R_D, C_{GS}, C_{GD}, C_{GB}, C_{DB}, C_{SB}\}$$

Physical Parameters

$$\{W, L, N_{RS}, N_{RD}, A_S, A_D, P_S, P_D\}$$

Models for Computer Simulation

MOS Transistor Models for SImulation

Physical Parameters

$$\{W, L, N_{RS}, N_{RD}, A_S, A_D, P_S, P_D\}$$

- Separate Process Part of Model from Instantiation part of Model
- Use one Process File for Entire Process and Specify only Physical Geometric Parameters for Each Device

Models for Computer Simulation

MOS Transistor Models for SImulation

Physical Parameters

$$\{W, L, N_{RS}, N_{RD}, A_S, A_D, P_S, P_D\}$$

MOS Models for Simulation

- Level 1
- Level 2
- Level 3
- BSIM 3
- BSIM 4
- PSP

Hierarchy Used in Models